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Utility Patent Application Transmittal
(Only for new non-provisional applications Under 37 CFR 1.53(b))

ASSISTANT COMMISSIONER FOR PATENTS
Washington, D. C. 20231

Case Docket No. 0325.00368
Date: August 3, 2000

Sir:

Transmitted herewith for filing is a patent application of:

Inventor(s): Steven P. Larky and Terry D. Little

For: ANALOG SIGNAL VERIFICATION USING DIGITAL SIGNATURES

Enclosed are:

1. X Specification (15 pages); Claims (6 pages); Abstract (1 page)

2. X 2 sheets of formal drawings.

3. X Oath or Declaration Total Pages 3
   a. X Newly executed (original or copy)
   b. ___ Copy from a prior application (37 CFR 1.63(d)) (for continuation/divisional with Item 5 completed)
   c. ___ Copy of Revocation of Previous Power

4. ___ Incorporation By Reference (usable if Item 3b is checked)
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Item 3b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

5. ___ If a Continuing Application, check appropriate box and supply the requisite information below and in a preliminary amendment:

___ Continuation _____ Divisional _____ Continuation-in-part (CIP)
of prior application no.: _____

6. X An assignment to CYPRESS SEMICONDUCTOR CORP. along with PTO form 1595.

7. ___ A PTO Form 1449 with a copy of the references not previously cited.

8. X Return Receipt Postcard

9. ___ Other:

The filing fee has been calculated as shown below:

	No. Filed	No. Extra	Fee	Amount
Basic Fee	--	--	--	$690.00
Total Claims	20	0	x $ 18.00	$ 0.00
Indep. Claims	3	0	x $ 78.00	$ 0.00
Mult. Dep. Claims			$260.00	$ 0.00

SUB-TOTAL $690.00

__ SMALL ENTITY STATUS (divide SUB-TOTAL by two) ...... $ ____

X Assignment Recordal Fee ($40.00) .... $ 40.00

TOTAL $730.00

X A check in the amount of $730.00 to cover the filing fee is enclosed.

X The Commissioner is hereby authorized to charge any fees under 37 CFR 1.16 and 1.17 which may be required by this paper or associated with this filing to Deposit Account No. 50-0541. A duplicate copy of this sheet is enclosed.

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Customer Number or Bar Code Label: **21363**

PATENT TRADEMARK OFFICE

CERTIFICATE OF EXPRESS MAILING

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being deposited with the United States Postal Service via Express Mail Label No. EL561050843US in an envelope addressed to: BOX PATENT APPLICATION, Assistant Commissioner for Patents, Washington, D.C. 20231, on August 3, 2000.

By: Mary Donna Berkley

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Respectfully submitted,

By ____________________

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ANALOG SIGNAL VERIFICATION USING DIGITAL SIGNATURES

Field of the Invention

The present invention relates to a method and/or architecture for analog signal verification generally and, more particularly, to a method and/or architecture for analog signal verification using digital signatures.

Background of the Invention

Conventional approaches for verifying analog signals either (i) run a full-chip analog simulation, subsetting the analog blocks into smaller design blocks, or (ii) run layout versus schematic (LVS) simulations during final processing stages.

Such conventional approaches have several disadvantages. A full-chip analog simulation is very time consuming, difficult to setup, and may not even be possible for large designs. For large designs, when applicable, smaller subsets of the design can be created. The design subsets can be of a manageable design size. The smaller design subsets generally can be fully simulated within an analog simulator. However, the design subset approach requires

extra, potentially error-inducing steps. The errors can be introduced in an effort to make a smaller design subset that includes all of the necessary functionality. Furthermore, the process of creating the smaller design subsets must be continually repeated, increasing the overall design effort.

LVS simulations can be implemented to verify analog connectivity. However, LVS simulators have severe drawbacks. Any errors found are expensive (in terms of decision schedule) to correct, since LVS simulation is implemented late in the file verification process. LVS only verifies a layout against a schematic. If the same error is introduced in both the schematic and the layout, the LVS approach will not detect the error.

Summary of the Invention

The present invention concerns a method for modeling analog signals that may comprise (A) detecting one or more attributed analog signals and (B) modeling the attributed analog signals by adding a signature to each of the one or more attributed analog signals.

The objects, features and advantages of the present invention include providing a method and/or architecture for analog

signal verification using digital signatures that may (i) be faster than analog simulation, (ii) be implemented without size constraints (e.g., compared to creating a subset of a design that may fit within an analog simulator), (iii) be implemented without continually rebuilding a subset, (iv) be implemented without requiring analog blocks to be completely held within an easily defined subset, (v) be compatible with a large number of analog blocks and an arbitrary mix of analog and digital blocks, (vi) locate a connection error early in the design process and/or (vii) provide verification of connections in a functional manner.

Brief Description of the Drawings

These and other objects, features and advantages of the present invention will be apparent from the following detailed description and the appended claims and drawings in which:

FIG. 1 is a block diagram of a preferred embodiment of the present invention; and

FIG. 2 is a flow diagram illustrating an exemplary operation of the present invention.

Detailed Description of the Preferred Embodiments

Referring to FIG. 1, a block diagram of a circuit (or system) 100 is shown in accordance with a preferred embodiment of the present invention. The system 100 generally comprises a source block (or circuit) 102 and a digital simulator block (or circuit) 104. The source block 102 may comprise a digital source block (or circuit) 106, an analog source block (or circuit) 108 and a create and add digital signature block (or circuit) 110. The system 100 may provide analog signal verification using digital signatures. The system 100 may be implemented to provide verification of analog signals in models. The system 100 may perform multiple tests to provide verification of the models. The system 100 may provide verification of analog signals in a functional manner, decreasing chances of a same error occurring in both a schematic and a layout of a particular design.

The digital source 106 may have an output 112 that may present a signal (e.g., DIGITAL). The signal DIGITAL may be presented to an input 114 of the digital simulator 104. The analog source 108 may have an output 116 that may present a signal (e.g., ANALOG). The signal ANALOG may be presented to an input 118 of the create and add digital signature block 110. The create and add

digital signature block 110 may have an output 120 that may present a signal (e.g., AN_D). The signal AN_D may be presented to an input 122 of the digital simulator 104. In one example, the signal AN_D may be implemented as an analog signal implemented with a digital signature. In another example, the signal AN_D may be implemented as an attributed analog signal. However, the signal AN_D may be implemented as another appropriate type signal in order to meet the criteria of a particular implementation. The digital simulator 104 may provide digital simulations of an analog design. The digital simulator 104 may provide digital simulations using digital signatures added to the signal ANALOG.

Referring to FIG. 2, a block diagram of a system (or process) 200 illustrating an operation of the present invention is shown. The system 200 may be implemented to provide verification of analog signals. The system 200 may be implemented to provide connectivity verification of the analog signals. The system 200 generally comprises a source block (or state) 202 and a destination block (or state) 204. The source block 202 may be configured to generate an analog signal attributed with a digital signature. The destination block 204 may be configured to determine a connectivity of the attributed analog signal.

The source block 202 generally comprises a receive block (or state) 204, an add block (or state) 206 and a create block (or state) 208. In one example, the receive block 204 may be implemented as a receive analog signal state, the add block 206 may be implemented as an add digital signature block and the create block 208 may be implemented as a create digital signature block. However, the receive block 204, the add block 206 and the create block 208 may each be implemented as another appropriate device or state in order to meet the criteria of a particular implementation.

The receive block 204 may present an analog signal to the add digital signature block 206. The add digital signature block 206 may add a digital signature to the analog signal. The digital signature may allow the system 200 to verify a connectivity of the analog signal. The digital signature may be generated by the create digital signature block 208. The digital signature block 208 may create an unique signature for each analog signal presented to the add digital signature block 206. The attributed analog signals (e.g., the analog signals each with an added digital signature) may be presented to the destination block 204.

The destination block 204 generally comprises a receive block (or state) 210, a verification decision block (or state) 212,

a processing block (or state) 214 and a disable block (or state) 216. In one example, the receive block 210 may be implemented as a receive attributed signal block and the processing block 214 may be implemented as a continue processing block. However, the receive block 210 and the processing block 214 may each be implemented as another appropriate device or state in order to meet the criteria of a particular implementation.

The receive block 210 may receive the attributed analog signal. The receive block 210 may present the attributed analog signal to the verification block 212. The verification block 212 may attempt to verify the digital signature of the analog signal. The verification block 212 may verify the digital signature to ensure proper functionality (e.g., connectivity). If the digital signature indicates proper functionality, the system 200 may continue processing of the analog signal in the block 214. If the digital signature indicates non-proper functionality, the system 200 may disable processing at the analog signal at the disable block 216. The verification block 212 may determine connectivity of the analog signal being processed.

The system 200 may implement the digital signature to check for another appropriate attribute and/or parameter. The

appropriate attributes and/or parameters may include applicable digital and/or analog parameters. The system 100 (or 200) may implement a particular number of pulses of different widths for each analog signal. Each pulse width may be applicable for a particular parameter. For example, the digital signature may be implemented as a number of multi-pulse width signals, indicating a required power supply, clock domain, etc.

The unique digital signature may be provided through a number of implementations such as (i) a varying frequency signal, (ii) a pulse of different width, (iii) a series of pulses of known width, etc. For example, a Verilog model of an analog design (or block) may be used to allow connectivity of the analog pins to be verified in a digital simulator.

The unique signatures may allow easier implementation of analog devices. Additionally, the system 100 (or 200) may allow ease of design overhead when implementing analog devices. The system 100 (or 200) may allow multiple current sources to be implemented to provide re-assurance that each sink is connected to a source signature (e.g., the unique digital signature). The digital signatures may be automatically generated without

additional user input. The digital signatures may allow a designer/user to verify connectivity of the analog signals.

The system 100 may provide an approach for verifying correct connectivity of analog signals within a digital simulation environment. The actual function of the analog signals cannot always be modeled within the digital simulator. However, it is generally desirable to verify the connectivity of the analog signals as early as possible in the design process. The system 100 may allow a user/designer to determine, early in the design process, connectivity of the analog signals. The system 100 may add digital signatures on analog ports. The system 50 generally adds a unique digital signature to each analog signal. The appropriate signature may be generated at a source and verified at a destination. The digital signature is generally output from an analog source and input to an analog destination. Such an implementation may allow the connectivity of the analog signals to be verified within a digital simulator.

The system 100 may allow Verilog models of analog blocks to be created as they normally would, modeling the function either behaviorally or functionally. The analog blocks may be inserted into a full-chip (or core) netlist as in a normal design process.

For all analog signals that do not have a digital version (e.g., a current source), a unique digital signature is generally assigned. Within the Verilog model, the signature is either generated or verified, depending on whether the digital signature is a source or a sink of the analog signal. In cases where the analog signal is a sink, if the expected signature is not received, then the function of the modeled analog block is disabled.

Where the analog signal is an output, the digital signature may be created within an analog model for a particular block. Where the analog signal is an input, the digital signature may be verified to ensure the connectivity is as expected. If the signal is not as expected, the function of the analog modeled block is generally disabled. The disabled analog modeled block may be easily detected in the digital simulator.

The system 100 may add an unique digital signature to an analog pin within a Verilog model of an analog block. The digital signature may allow a connectivity of the analog pin to be verified in a digital simulator. The system 100 may allow a non-analog savvy engineer to easily implement analog blocks.

The system 100 may be implemented to verify the connectivity and correctness of analog circuitry within a complex

logic design. The system 100 may create an unique digital signature for each unique analog source and add code to a model of an analog block to cause the unique signature to be generated within a digital simulator. The added code may be implemented to allow the digital simulator to detect and verify the unique digital signature. The system 100 may allow a digital simulator to verify a correct connectivity of an analog signal within a digital simulator. The system 100 may allow a digital simulator to verify that a number of analog signals have been correctly connected.

The system 100 may reduce errors related to integration of analog intellectual property (IP). The system 100 may allow ease of analog IP implementation. The value of the system 100 may grow as more analog IP is reused and the original designers are not as involved. Furthermore, the system 100 may be implemented for electronic design automation (EDA) tool companies.

The system 100 (or 200) may be faster than analog simulation. The system 100 may have no size constraints (e.g., compared to creating a subset of the design that may be required to fit within an analog simulator). The system 100 may not be required to continually rebuild an analog subset. The system 100 may not require the analog blocks (e.g., devices) to be completely

held within an easily defined subset. The system 100 may be compatible with a large number of analog blocks and an arbitrary mix of analog and digital blocks.

Additionally, the system 100 may determine connection errors at an earlier processing time saving valuable resources. The system 100 may verify the analog connections in a functional manner, decreasing the chances of a same error occurring in both the schematic and the layout of the device.

The following is an example of Verilog source files that may be used to implement the present invention:

```
// Analog signature pulse generator for use with test_sig.v
module gen_sig (signature);
output signature;
reg signature;
parameter ref_num = 0;
initial begin
   signature = 0;
   #(ref_num + 100) signature = !signature;
   $display("signature %0d high, %t", ref_num, $time);
   #(ref_num * 2 + 200) signature = !signature;
   $display("signature %0d low, %t", ref_num, $time);
end
endmodule
```

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```
// Analog signature pulse checker for use with gen_sig.v
module test_sig (signature, error);
input    signature;
output   error;
reg      error;
parameter ref_num = 0;
integer  edge_det;
initial begin
   error = 0;
   edge_det = 0;
   $display("Initialize current source checker %0d", ref_num);
end
always @(signature) begin
   $display("Test Signature %0d, = %b", ref_num, signature);
end
initial begin : CHECK
   #50;
   @(posedge signature) begin
      edge_det = 1;
      #(ref_num * 2 + 200) if ( !signature ) begin
         $display("ERROR: on current source %0d signature low,
expected high :ERROR", ref_num);
         error = 1;
      end
      #1 if ( signature ) begin
```

```
            $display("ERROR: on current source %0d signature high
expected low :ERROR", ref_num);
            error = 1;
         end
         if (!error)
            $display("VERIFIED: Current source %0d signature
:VERIFIED, %t", ref_num, $time);
         disable EDGE_DET;
      end
   end
   initial begin : EDGE_DET
      #(ref_num + 150) if (!edge_det) begin
         $display("ERROR: Signature check END on %0d, NO SIGNATURE
DETECTED :ERROR", ref_num);
         disable CHECK;
      end
   end
   endmodule
```

The function performed by the flow diagram of FIG. 2 may be implemented using a conventional general purpose digital computer programmed according to the teachings of the present specification, as will be apparent to those skilled in the relevant art(s). Appropriate software coding can readily be prepared by skilled programmers based on the teachings of the present

disclosure, as will also be apparent to those skilled in the relevant art(s).

The present invention may also be implemented by the preparation of ASICs, FPGAs, or by interconnecting an appropriate network of conventional component circuits, as is described herein, modifications of which will be readily apparent to those skilled in the art(s).

The present invention thus may also include a computer product which may be a storage medium including instructions which can be used to program a computer to perform a process in accordance with the present invention. The storage medium can include, but is not limited to, any type of disk including floppy disk, optical disk, CD-ROM, and magneto-optical disks, ROMs, RAMs, EPROMs, EEPROMs, Flash memory, magnetic or optical cards, or any type of media suitable for storing electronic instructions.

While the invention has been particularly shown and described with reference to the preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and details may be made without departing from the spirit and scope of the invention.

CLAIMS

1. A method for modeling analog signals comprising the steps of:

(A) detecting one or more attributed analog signals; and

(B) modeling said attributed analog signals by adding a signature to each of said one or more attributed signals.

2. The method according to claim 1, wherein step (B) further comprises:

performing digital simulations with said one or more attributed analog signals.

3. The method according to claim 1, wherein each of said one or more signatures corresponds to a predetermined parameter.

4. The method according to claim 1, wherein each of said one or more signatures comprises an unique digital signature.

5. The method according to claim 1, wherein step (B) further comprises:

performing verification of said one or more attributed analog signals.

6. The method according to claim 1, wherein step (B) further comprises:

determining a connectivity of said one or more attributed analog signals.

7. The method according to claim 1, wherein step (B) further comprises:

verifying a model of an analog block configured to receive at least one of said one or more attributed analog signals.

8. The method according to claim 7, wherein step (B) further comprises:

verifying a second one or more models of analog blocks configured to receive another at least one of said one or more attributed analog signals.

9. A method for testing a model of a device, comprising the steps of:

(A) performing tests on said model; and

(B) verifying connectivity of one or more attributed analog signals within said model by verifying one or more signatures associated with each of said one or more attributed analog signals.

10. The method according to claim 9, wherein step (B) further comprises:

if said one or more attributed analog signals are not verified, disabling said device.

11. The method according to claim 9, wherein step (B) further comprises verifying a model of an analog block configured to receive at least one of said one or more attributed analog signals.

12. The method according to claim 11, wherein step (B) further comprises verifying a second one or more models of analog blocks configured to receive another at least one of said one or more attributed analog signals.

13. A method for verifying a model of a device comprising the steps of:

(A) detecting one or more attributed analog signals; and

(B) performing one or more verifications of one or more predetermined parameters in response to said one or more attributed analog signals.

14. The method according to claim 13, wherein step (A) further comprises:

adding a signature to at least one of said one or more attributed analog signals.

15. The method according to claim 14, wherein said signature comprises an unique digital signature.

16. The method according to claim 13, wherein said one or more predetermined parameters comprise one or more digital parameters.

17. The method according to claim 13, wherein said one or more predetermined parameters comprise one or more analog parameters.

18. The method according to claim 13, wherein step (B) further comprises determining a connectivity of said one or more attributed analog signals.

19. The method according to claim 13, wherein step (B) further comprises verifying a model of an analog block in response to said one or more attributed analog signals.

20. The method according to claim 13, wherein step (A) further comprises:

adding a first signature to at least one of said one or more attributed analog signals; and

adding a second signature to said at least one attributed analog signal, wherein said first signature corresponds to a first predetermined parameter of said one or more predetermined parameters and said second signature corresponds to a second

predetermined parameter of said one or more predetermined parameters.

ABSTRACT OF THE DISCLOSURE

A method for modeling analog signals that may comprise (A) detecting one or more attributed analog signals and (B) modeling the attributed analog signals by adding a signature to each of the one or more attributed analog signals.

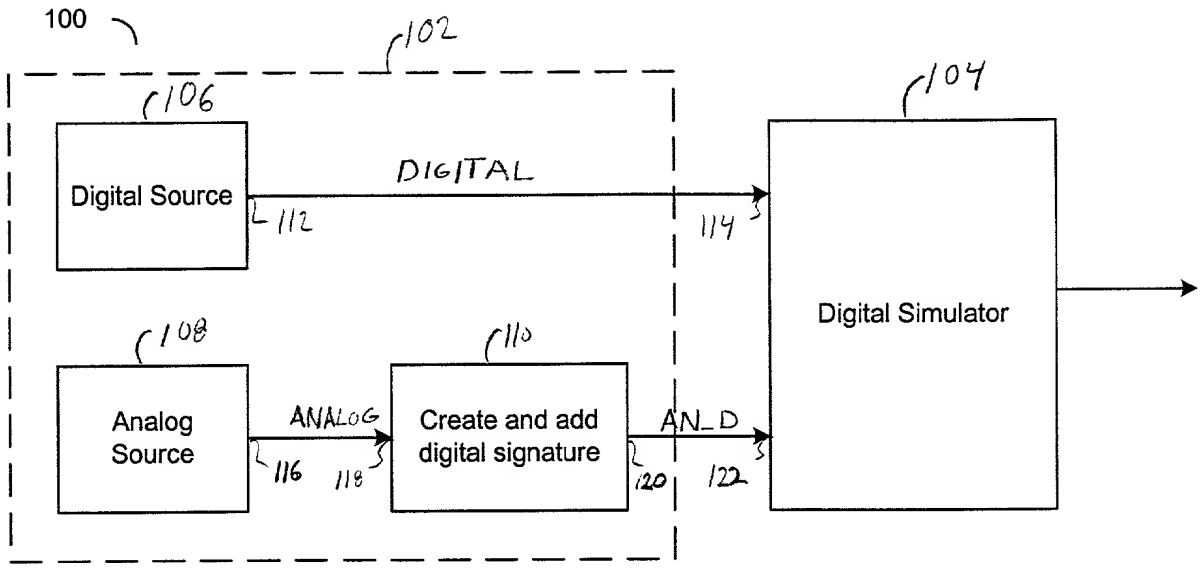
100
102
104
106
108
110
Digital Source
DIGITAL
112
114
Digital Simulator
Analog Source
ANALOG
116
118
Create and add digital signature
AN_D
120
122

FIG. 1

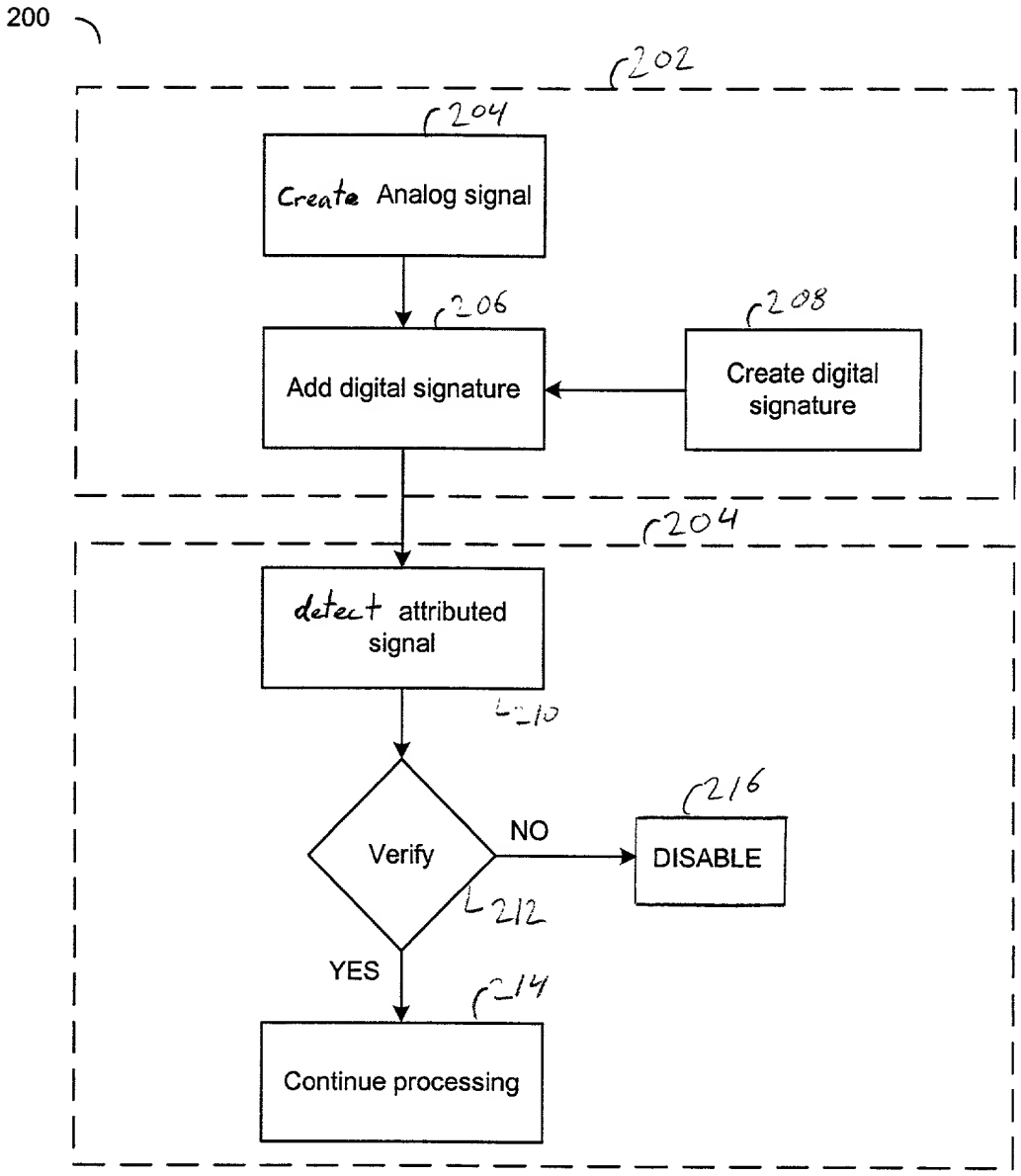
200
202
204
Create Analog signal
206
Add digital signature
208
Create digital signature
204
detect attributed signal
210
Verify
NO
216
DISABLE
212
YES
214
Continue processing

FIG. 2

Docket No. 0325.00368

DECLARATION, POWER OF ATTORNEY AND PETITION

We, the undersigned inventors, hereby declare that:

My residence, post office address and citizenship are given next to my name;

We believe that we are the first, original and joint inventors of the subject matter claimed in the application for patent entitled **"ANALOG SIGNAL VERIFICATION USING DIGITAL SIGNATURES"**, which:

__X__ is submitted herewith;

_____ was filed on _____ as Application Serial No. _____ and amended on _____;

We have reviewed and understand the contents of the above-identified application for patent (hereinafter, "this application"), including the claims;

We acknowledge the duty under Title 37, Code of Federal Regulations, Section 1.56, to disclose to the United States Patent and Trademark Office information known to be material to the patentability of this application. We also acknowledge that information is material to patentability when it is not cumulative to information already provided to the United States Patent and Trademark Office and when it either

> compels, by itself or in combination with other information, a conclusion that a claim is unpatentable under the preponderance of evidence standard, giving each term in the claim its broadest reasonable construction consistent with the application, and before any consideration is given to evidence which may be submitted to establish a contrary conclusion of patentability, or
>
> refutes or is inconsistent with a position taken in either (i) asserting an argument of patentability, or (ii) opposing an argument of unpatentability relied on by the United States Patent and Trademark Office;

We hereby claim the priority benefit under Title 35, Section 119(e), of the following United States provisional patent applications:

Application No.	Filing Date

We hereby claim the priority benefit under Title 35, Section 120, of the following United States patent applications:

Serial No.	Filing Date	Status

Docket No. 0325.00368

We hereby claim the priority benefit under Title 35, Section 365(c), of the following PCT International patent applications designating the United States:

Application No.	Filing Date

Where the subject matter of the claims of this application is not disclosed in the United States or PCT priority patent applications identified above, we acknowledge the duty to disclose information known to be material to the patentability of this application that became available between the filing dates of this application and of the priority United States or PCT patent applications.

We hereby appoint as our attorneys with full power of substitution to prosecute this application and conduct all business in the United States Patent and Trademark Office associated with this application: Customer No. 021363.

21363

PATENT TRADEMARK OFFICE

We declare that all statements made herein of our own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of this application or any patent issuing thereon.

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Signature of First Joint Inventor

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Docket No. 0325.00368

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